

Application No.: 10/675,039
Reply to Office Action of July 28, 2005

REMARKS/ARGUMENTS

Request for Interview

Applicant requests an oral interview with the Examiner prior to the Examiners issuing any rejection of the claims in the patent application.

Applicant refers the Examiner to the following points:

I. IT IS FIRST NOTED THAT THE CACHE MEMORY MANAGER IS ADAPTED TO RECEIVE QUERIES FROM THE PLURALITY OF DIRECTORS.

II. THE CACHE MEMORY MANAGER IS SEPARATE FROM THE CACHE MEMORY.

III. IT IS ALSO NOTED THAT THE FOLLOWING FOUR ELEMENTS ARE ALL INTERCONNECTED ARE INTERCONNECTED THROUGH A PACKET SWITCHING NETWORK:

1. THE CACHE MEMORY MANAGER;
2. THE PLURALITY OF FRONT END DIRECTORS;
3. THE PLURALITY OF BACK END DIRECTORS; AND,
4. THE CACHE MEMORY

As set forth on page 8, beginning at line 14 through line 22: Referring now to FIG. 2, a data storage system 100 is shown for transferring data between a host computer/server 120 and a bank of disk drives 140 through a system interface 160. The system interface 160 includes: a plurality of, here 32 front-end directors 180₁-180₃₂ coupled to the host computer/server 120; a plurality of back-end directors 200₁-200₃₂ coupled to the bank of disk drives 140; a data transfer section 240, having a global cache memory 220, coupled to the plurality of front-end directors 180₁-180₁₆ and the back-end directors 200₁-200₁₆; a messaging network 260, operative independently of the data transfer section 240, coupled to the plurality of front-end directors 180₁-180₃₂ and the plurality of back-end directors 200₁-200₃₂, as shown; and, a cache memory manager 265.

As pointed out on page 9, line 19 through page 10, line 6: The cache memory manager 265 includes therein a memory 267 for storing a map maintaining a relationship

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between data stored in the cache memory 220 and data stored in the bank of disk drives 240. The cache memory manager 265 also includes a CPU coupled to the message network 260 and a memory controller 270 coupled between the CPU 268 and the memory 267, as shown. Further detail of the cache memory manager 265 and the message network 260 are provided herein in connection with FIG. 6. Suffice it to say here, however, that the cache memory manager 265 provides an interface between the host computer 102, the bank of disk drives 104, and the cache memory 220 via the message network 260 for determining for the front end directors 180₁-180₃₂ and back-end directors 200₁-200₃₂ whether data to be read from the bank of disk drives 104, or data to be written to the bank of disk drives 104, resides in the cache memory 220. The memory controller 270 contains hardware to assist in the management functions, including Content Addressable functions, to search the lists; and Indirect Addressing capability, to work linked lists and queues.

With such cache memory manager 265, the cache memory 220 in the data transfer section is not burdened with the task of transferring the director messaging but rather a messaging network is provided, operative independent of the data transfer section, for such messaging thereby increasing the operating bandwidth of the system interface.

As pointed out on page 18, lines 5 through line 9: The front-end and back-end directors 18₁-18₄, 20₁-20₄ and the global cache memory communicate with one another through a packet switching network. The packet switching network includes crossbar switches 32 coupled to each one the directors, as shown, and a packet switching network section 26. The cache memory manager 265 is interconnected to the packet switching network via the packet switching network section 26.

Thus, from the above it is noted that the cache memory manager 265 is SEPARATE from the cache memory 220.

Grounds of Rejection to be Reviewed

Whether claims 1-6 are unpatentable under 35 U. S. C. 103 as being obvious over Dobecki (U. S. Patent No. 6,611,879 in view of Armilli et al. (Published U. S. Patent Application 2003/0009643)).

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Argument:

Claim 1 points out that the system includes:

a cache memory manager, adapted to receive queries from the plurality of directors, such cache memory manager having therein a memory for storing a map maintaining a relationship between data stored in the cache memory and data stored in the disk drives;

wherein the cache memory manager receives the queries from the plurality of directors and operates independently of the plurality of directors in processing such queries to determine for the querying directors whether data to be read from the disk drives, or data to be written to the disk drives, resides in the cache memory;

a packet switching network; and

wherein the cache memory manager, plurality of front end directors, plurality of back end directors and cache memory are interconnected through the packet switching network. (emphasis added)

With regard to points I and II above:

It is respectfully submitted that Arimilli et al., describes a system wherein the cache memory manager is included within the cache memory. Further, in Arimilli et al., since the cache memory manager, is included within the cache memory, the cache memory manager of Arimilli et al. is not adapted to receive queries from the plurality of directors.

The Examiner recognizes that Dobecki does not describe a cache memory manager as claimed but takes the position that it would be obvious to "include a cache memory manager as that of Arimilli et al. in the system of Dobecki...". Assuming *arguendo* that one would "include a cache memory manager as that of Arimilli et al. in the system of Dobecki, the resulting system would have the cache memory manager of within the cache memory. That is, referring to Applicant FIG. 2, the resulting system suggested by the Examiner would have the cache memory manager 265 within the cache memory 220. Such an arrangement would be contrary to the featured described above "

With regard to point III above:

Referring to the claims, it is noted that claim 1 points out the system includes a packet switching network and that the system includes that four elements (i.e., (1) the cache memory manager; (2) the plurality of front end directors; (3) the plurality of back end

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directors; and (4) the cache memory interconnected through the packet switching network. With the system suggested above, (i.e., one where the cache memory manager 265 is within the cache memory 220) all four elements set forth above would not be connected to the common packet switching network because the cache memory manager would be within the cache memory.

Claim 7 points out that that the system includes:

a cache memory manager having a processor, adapted to receive and process queries from the plurality of directors, such cache memory manager having therein a memory for storing a map maintaining a relationship between data stored in the cache memory and data stored in the disk drives;

...
wherein the cache memory manager is separate from the cache memory and

wherein the, plurality of front end directors, plurality of back end directors and cache memory are interconnected through the packet switching network.

As noted above, with the system suggested above, (i.e., one where the cache memory manager 265 is within the cache memory 220) the cache memory would not be separate from the cache memory.

In the event a petition for extension of time is required by this paper and not otherwise provided, such petition is hereby made and authorization is provided herewith to charge deposit account No. 05-0889 for the cost of such extension.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 05-0889.

Respectfully submitted,



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10-27-2005
Date